UNIVAC 1219 COMPUTER

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GENERAL CHARACTERISTICS

The UNIVAC® 1219 Computer is a medium scale, general purpose computer. It is a faster version of the widely-used UNIVAC 1218 Computer and is functionally compatible with it. It is an advanced military computer designed to comply with the environmental specifications of MIL-E-16400.

The UNIVAC 1219 Computer is an 18-bit digital computer capable of transferring 500,000 words per second. It is equipped with a 2-microsecond MAIN Memory and features a 500-nanosecond CONTROL Memory. It can be supplied with 16 full-duplex I/O channels where each channel is associated with a complete set of program interrupts. It is equipped with an external synchronizer function in addition to an automatic addressable clock cell. The UNIVAC 1219 Computer has been designed to provide a complete, straightforward interface enabling easy adaptation to the requirements of a system rather than requiring modification of the system to accommodate the computer.

TECHNICAL CHARACTERISTICS

MEMORY

Control Memory

Cycle Time:	500 nanoseconds
Capacity:	64 or 96 18-bit words
Type:	Word organized, magnetic core
Purpose:	Index registers, clock cells, I/O buffer control registers; operates in the "shadow" of the Main Memory at a 4:1 ratio.

Main Memory

Cycle Time:	2 microseconds
Capacity:	4096, 8192, 16,384, or 32,768 18-bit words (standard options)
Type:	Coincident current, magnetic core
Purpose:	I/O interrupt registers, program and data storage.

NDRO Memory

Cycle Time:	2 microseconds
Capacity:	32 18-bit words
Type:	Word organized, magnetic core, unalterable
Purpose:	Bootstrap (initial load) program storage. Programs available for paper tape and magnetic tape load.

INPUT/OUTPUT

Channels

Type:	Simplex, 18-bit parallel
Number:	32 maximum; 16 Input plus 16 Output
Transfer Rate:	One channel — 166,000 18-bit words/second (maximum) Multi-channel — 500,000 18-bit words/second (maximum)
Operation:	Each channel fully buffered and once activated operates without program attention, asynchronous, at the rate of the peripheral unit.

Information Transfers

Input Channels:	Input data, interrupt data
Output Channels:	Output data, external command data
Processing Time Required:	2 microseconds/word transferred 0 microseconds during extended sequence instructions
Delay due to Program:	2 microseconds (maximum)

Operating Modes (Standard)

Normal Single Channel: 18-bit parallel transfers

Normal Dual Channel: Consecutive (even/odd numbered) channels may be "paired" to form a single 36-bit parallel channel.

Externally Specified Index (Dual Channel):
18-bit parallel data transfers with storage address indirectly specified by external device; useful for multiplexing/decommutating data to/from computer.

Externally Specified Address (Dual Channel):
18-bit parallel data transfers with storage address directly specified by external device.

Intercomputer Single Channel:
Direct 18-bit parallel data transfers with other UNIVAC computers; no interface adapters required for intercomputer communication.

Intercomputer Dual Channel:
Direct 36-bit parallel data transfer with other UNIVAC Computers. No interface adapters required for intercomputer communication.

Interrupts

Input Channels: 16 external interrupts plus 16 internal interrupts (programmer option)

Output Channels: 16 internal interrupts (programmer option)

CONTROL

Instructions

Type: Single Address

Address Modification via: 8 Control-Memory-contained index registers.

Repertoire: 96 instructions

Clock

Type: Automatic, additive, under program control

Location: Control Memory

Duration: Established under program control

Granularity: LSB represents 1/1024 second

Interrupt: Interrupt occurs when program pre-set value is reached.

Synchronizer

Interrupt: Interrupt occurs whenever the non-I/O synchronizing control line is set to logical one by an external device.

Purpose: To allow a variable-granularity clock function or to provide a high priority alarm recognition capability.

ARITHMETIC

Organization:	18-bit parallel, one's complement, integer
Execution Times:	Typical execution times, including instruction and data fetch plus indexing.

Add, Subtract (single length)	4 μsec
Multiply/Divide	16 μsec
Add, Subtract (double length)	6 μsec
Compare/Masked Compare and Branch	6 μsec
Register shifts: right, left, single, double	2 + .5n μsec (n = shift count)

ENVIRONMENTAL REQUIREMENTS

General Requirements:	MIL-E-16400D (Navy)
Interference:	MIL-I-16910A
Enclosure:	MIL-STD-108D
Shock:	MIL-S-901
Vibration:	MIL-STD-167
Temperature:	0 degree to 50 degrees C
Humidity:	To 95 percent

POWER REQUIREMENTS

115 volt ± 10 percent, 1-phase, 60 cps, 150 watts maximum

115 volt ± 10 percent, 3-phase, 400 cps, 1500 watts maximum

SOFTWARE

Existing UNIVAC 1218 Subroutines

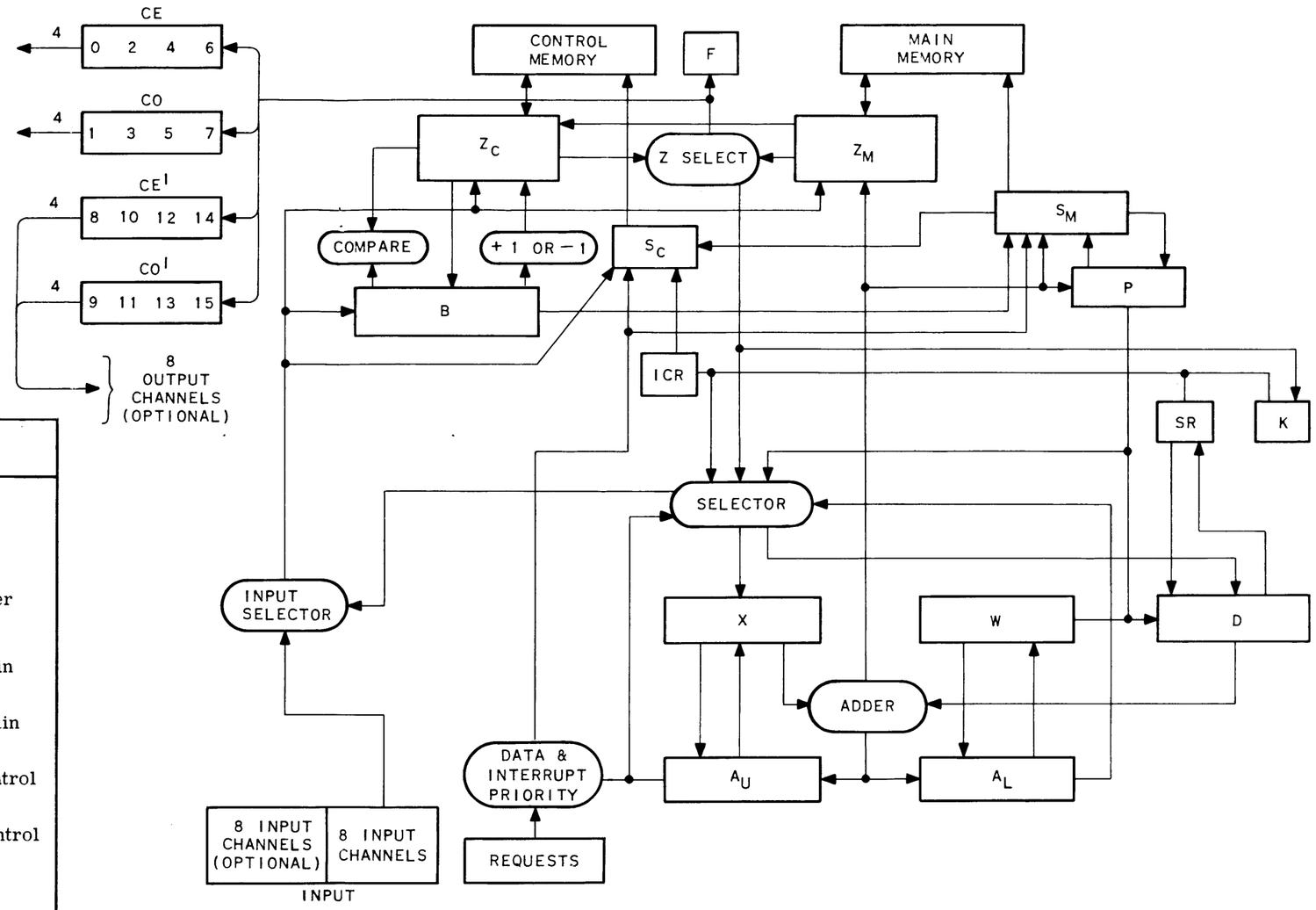
TRIM I

TRIM II

TRIM III

REGISTERS

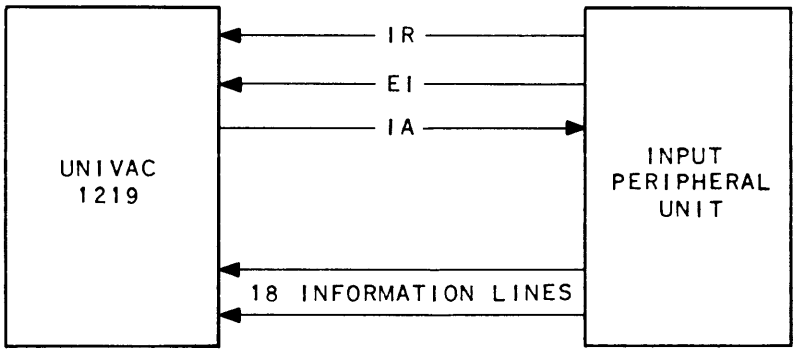
ID	SIZE (BITS)	FUNCTION
AL	18	Accumulator, Lower
AU	18	Accumulator, Upper
SR	4	Special Register
ICR	3	Index Control Register
P	15	Program Address
Sm	15	Storage Address, Main Memory
ZM	18	Storage Transfer, Main Memory
Sc	7	Storage Address, Control Memory
Zc	18	Storage Transfer, Control Memory
D	18	Data Transient
X	18	Exchange Transient
W	18	Auxiliary Arithmetic
CO	18	Output Buffer, Channels 0, 2, 4, 6
CE	18	Output Buffer, Channels 1, 3, 5, 7
CO'	18	Output Buffer, Channels 8, 10, 12, 14 (OPT)
CE'	18	Output Buffer, Channels 9, 11, 13, 15 (OPT)
B	18	Data Transient



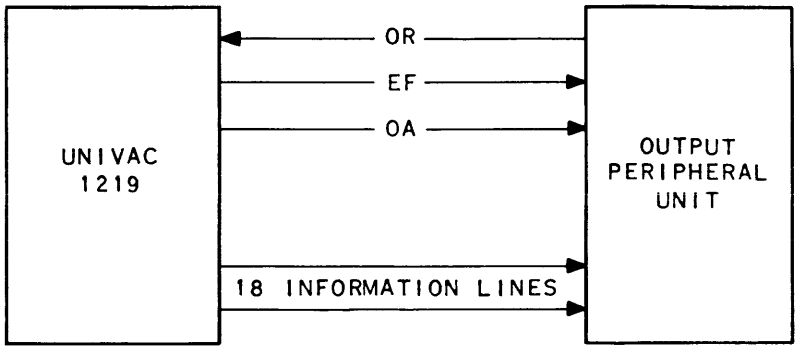
PRELIMINARY BLOCK DIAGRAM
UNIVAC 1219 COMPUTER

DESCRIPTION OF INPUT/OUTPUT CONTROL SIGNALS

	Signal Name	Origin	Meaning
Input Channel	Input Request (IR)	Peripheral Equipment	"I have a data word on the input lines ready for you to accept."
	Input Acknowledge (IA)	Computer	"I have sampled the word on the input lines."
	External Interrupt (EI)	Peripheral Equipment	"I have an Interrupt Code word on the input lines ready for you to accept."
Output Channel	Output Request (OR)	Peripheral Equipment	"I am in a condition to accept a word of data from you."
	Output Acknowledge (OA)	Computer	"I have put a data word for you on the output lines; sample them now."
	External Function (EF)	Computer	"I have put an External Function message for you on the output lines; sample them now."



ONE 1219 INPUT CHANNEL



ONE 1219 OUTPUT CHANNEL

ASSIGNED MEMORY ADDRESS

CONTROL MEMORY (Standard)

00000	Fault Register
00001-00010	8 Index Registers
00011	Real-Time Clock Interrupt Register
00012-00013	UNASSIGNED
00014-00015	Real-Time Clock Cells
00016	Synchronizing Interrupt Register
00017	Scale Factor Shift Count
00020-00037	UNASSIGNED
00040-00057	Output Buffer Control Registers (Channels 0-7)
00060-00077	Input Buffer Control Registers (Channels 0-7)

Optional with UNIVAC 1219 Computers equipped with 16 I/O)

00240-00257	Output Buffer Control Registers (Channels 8-15)
00260-00277	Input Buffer Control Register (Channels 8-15)

MAIN MEMORY

00100-00117	External Interrupt Registers (Channels 0-7)
00120-00137	UNASSIGNED
00140-00157	Output Monitor Registers (Channels 0-7)
00160-00177	Input Monitor Registers (Channels 0-7)
00300-00317	External Interrupt Registers (Channels 8-15)
00320-00337	UNASSIGNED
00340-00357	Output Monitor Registers (Channels 8-15)
00360-00377	Input Monitor Registers (Channels 8-15)
00400-177777	UNASSIGNED

NDRO MEMORY

00200-00237	Bootstrap Program

UNIVAC 1219 COMPUTER
REPERTOIRE OF INSTRUCTIONS

Code	Symbol	Description	Time μs
02	CMAL	Compare Y	4
03	CMALB	Compare Y + B	4
04	SLSU	Selective Substitute	4
05	SLSUB	Selective Substitute Y + B	4
06	CMSK	Masked Compare Y	4
07	CMSKB	Masked Compare Y + B	4
10	ENTAU	Enter AU, Y	4
11	ENTAUB	Enter AU, Y + B	4
12	ENTAL	Enter AL, Y	4
13	ENTALB	Enter AL, Y + B	4
14	ADDAL	Add Y, 18 bit	4
15	ADDALB	Add Y + B, 18 bit	4
16	SUBAL	Subtract Y, 18 bit	4
17	SUBALB	Subtract Y + B, 18 bit	4
20	ADDA	Add Y, 36 bit	6
21	ADDAB	Add Y + B, 36 bit	6
22	SUBA	Subtract Y, 36 bit	6
23	SUBAB	Subtract Y + B, 36 bit	6
24	MULAL	Multiply Y	16
25	MULALB	Multiply Y + B	16
26	DIVA	Divide, Y	16
27	DIVAB	Divide, Y + B	16
30	IRJP	Indirect RJP, Y	6
31	IRJPB	Indirect RJP, Y + B	6
32	ENTB	Enter B, Y	4
33	ENTBB	Enter B, Y + B	4
34	JP	Jump, Y	2
35	JPB	Jump, Y + B	2
36	ENTBK	Enter, B, U	2
37	ENTBKB	Modify B,U	2
40	CL	Store Zero, Y	4
41	CLB	Store Zero, Y + B	4
42	STRB	Store, B, Y	4
43	STRBB	Store B, Y + B	4
44	STRAL	Store AL, Y	4
45	STRALB	Store AL, Y + B	4
46	STRAU	Store AU, Y	4
47	STRAUB	Store AU, Y+ B	4
51	SLSET	Selective Set (IOR), Y	4
52	SLCL	Selective Clear (AND), Y	4
53	SLCP	Selective Complement (XOR), Y	4
54	IJPEI	Indirect Jump (RIL), Y	4
55	IJP	Indirect Jump, Y	4
56	BSK	Increment B, Skip, Y	4
57	ISK	Decrement Index, Skip, Y	6
60	JPAUZ	Jump AU Zero, Y	2
61	JPALZ	Jump AL Zero, Y	2
62	JPAUNZ	Jump AU Not Zero, Y	2
63	JPALNZ	Jump AL Not Zero, Y	2
64	JPAUP	Jump AU Positive, Y	2
65	JPALP	Jump AL Positive, Y	2
66	JPAUNG	Jump AU Negative, Y	2
67	JPALNG	Jump AL Negative, Y	2
70	ENTALK	Enter AL, Y	2
71	ADDALK	Add U, 12 bits	2
72	STRICR	Store ICR, Y	4
73	BJP	Decrement B, Jump, Y	2
74	STRADR	Store Address, Y	4
75	STRSR	Store SR, Deactivate SR, Y	4
76	RJP	Return Jump, Y	4
5011	IN	Initiate Input Buff, k	6
5012	OUT	Initiate Output Buff, k	6
5014	ERTCLK	Enable Real-Time Clock	2
5015	INSTP	Terminate Input, k	2
5016	OUTSTP	Terminate Output, k	2
5020	SRSM	Set Resume ff (Intercomp)	2
5021	SKPIIN	Skip Input Inact, k	2
5022	SKPOIN	Skip Output Inac, k	2
5024	WRFI	Wait for Interrupt	2
5026	OUTOV	Force Output One Word, k	2
5027	EXFOV	Force Ext Function One Word, k	2
5030	RIL	Remove Interrupt Lockout	2
5032	EXL	Remove Ext Interrupt Lockout	2
5034	SIL	Set Interrupt Lockout	2
5036	SXL	Set Ext Interrupt Lockout	2
5041	RSHAU	Right Shift AU, k	2+.5k
5042	RSHAL	Right Shift AL, k	2+.5k
5043	RSHA	Right Shift A, k	2+.5k
5044	SF	Scale A Left, k, SF	4+.5k
5045	LSHAU	Left Shift AU, k	2+.5k
5046	LSHAL	Left Shift AL, k	2+.5k
5047	LSHA	Left Shift A, k	2+.5k
5050	SKP	Skip Console Key, k	2
5051	SKPNBO	Skip No Borrow	2
5052	SKPOV	Skip Overflow	2
5053	SKPNOV	Skip No Overflow	2
5054	SKPODD	Skip L(AU,AL) Odd Parity	2
5055	SKPEVN	Skip L(AU,AL) Even Parity	2
5056	STOP	Stop Console Key, k	2
5057	SKPNR	Skip Resume ff (Intercomp)	2
5060	RND	Round AU	2
5061	CPAL	Complement AL	2
5062	CPAU	Complement AU	2
5063	CPA	Complement A	2
5072	ENTICR	Enter ICR, k	2
5073	ENTSR	Enter SR, k	2

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